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	Filing Date		2006-03-30	
	First Named Inventor	Rao Rajashekhar		
	Art Unit			
	Examiner Name			
Attorney Docket Number		1438.113.101/F02P041WOUS		

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	1	"A Pseudo Multi-Bank DRAM with Categorized Access Sequence", Shinichiro Shiratake, et al., 1999 Symposium on VLSI Circuits Digest of Technical Papers pp 127-130	<input type="checkbox"/>

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